



(19)

(11) Publication number:

**57199**

Generated Document.

**PATENT ABSTRACTS OF JAPAN**(21) Application number: **56085098**(51) Int'l. Cl.: **G06F 7/52**(22) Application date: **03.06.81**

(30) Priority:

(43) Date of application  
publication: **06.12.82**(84) Designated contracting  
states:(71) Applicant: **FUJITSU LTD**(72) Inventor: **SUGIURA SATOSHI**

(74) Representative:

**(54) MULTIPLYING DEVICE**

(57) Abstract:

**PURPOSE:** To simplify a Wallace tree circuit to make the operation cycle high-speed, by inputting the carry and the sum of the Wallace tree circuit to an adder and adding them to the preceding output of the adder to obtain a product value and performing only the addition of partial products in the tree circuit.

**CONSTITUTION:** A multiplier 12 and a multiplicand 10 are multiplied in a multiplying circuit 14, and an output A is applied to a Wallace tree circuit 16, and a carry output B' and a sum output C' from the circuit 16 are applied to an adder 26. A part F (lower 2 bits omitted) of the preceding addition output from a register 28 is inputted to the adder 26. The preceding output and the carry output B' and the sum output C' from the circuit 16 are added in the adder 26 to obtain a product value, and only the addition of partial products is performed in the circuit 26, and integral products and partial product results are added in the adder 26, thus

simplifying the circuit 16 to make the operation cycle high-speed.

COPYRIGHT: (C)1982,JPO&Japio

